

## 150 mA, 28V LDO Regulator With Shutdown

### Features:

- 150 mA Output Current
- Low Dropout Voltage, 260 mV Typical @ 20 mA,  $V_R = 3.3V$
- 50  $\mu A$  Typical Quiescent Current
- 0.01  $\mu A$  Typical Shutdown Current
- Input Operating Voltage Range: 2.0V to 28.0V
- Standard Output Voltage Options (1.8V, 2.5V, 3.0V, 3.3V, 5.0V, 10.0V, 12.0V)
- Output Voltage Accuracy:  $\pm 2\%$
- Output Voltages from 1.8V to 18.0V in 0.1V Increments are Available upon Request
- Stable with Ceramic Output Capacitors
- Current Limit Protection with Current Foldback
- Shutdown Pin
- High PSRR: 50 dB Typical @ 1 kHz

### Applications:

- Cordless Phones, Wireless Communications
- PDAs, Notebook and Netbook Computers
- Digital Cameras
- Microcontroller Power
- Car Audio and Navigation Systems
- Home Appliances

### Related Literature:

- AN765, "Using Microchip's Micropower LDOs" (DS00765), Microchip Technology Inc., ©2002
- AN766, "Pin-Compatible CMOS Upgrades to BiPolar LDOs" (DS00766), Microchip Technology Inc., ©2002
- AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), Microchip Technology Inc., ©2001

### Description:

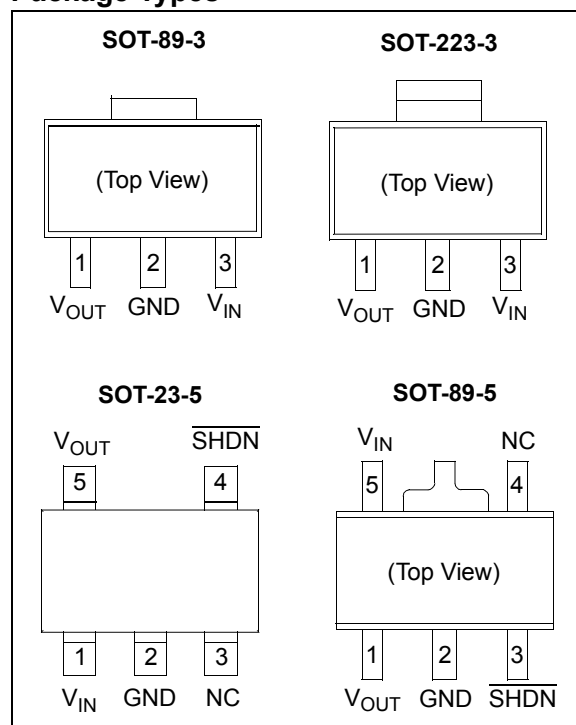
The MCP1804 is a family of CMOS low dropout (LDO) voltage regulators that can deliver up to 150 mA of current while consuming only 50  $\mu A$  of quiescent current (typical,  $1.8V \leq V_{OUT} \leq 5.0V$ ). The input operating range is specified from 2.0V to 28.0V.

The MCP1804 is capable of delivering 100 mA with only 1300 mV (typical) of input to output voltage differential ( $V_{OUT} = 3.3V$ ). The output voltage tolerance of the MCP1804 at  $+25^\circ C$  is a maximum of  $\pm 2\%$ . Line regulation is  $\pm 0.15\%$  typical at  $+25^\circ C$ .

The LDO input and output are stable with 0.1  $\mu F$  of input and output capacitance. Ceramic, tantalum or aluminum electrolytic capacitors can all be used for input and output. Overcurrent limit with current foldback to 40 mA (typical) provides short circuit protection. A shutdown (SHDN) function allows the output to be enabled or disabled. When disabled, the MCP1804 draws only 0.01  $\mu A$  of current (typical).

Package options include the 3-lead SOT-89, 3-lead SOT-223, 5-lead SOT-23 and 5-lead SOT-89.

### Package Types



\_\_\_\_\_

The block diagram illustrates the internal control system of the DC-DC converter. The input voltage  $V_{IN}$  is connected to the input of the converter, which includes a diode and a MOSFET. The output voltage  $V_{OUT}$  is taken from the output of the converter, which includes a diode and a MOSFET. The control system consists of a Shutdown Control block, a Voltage Reference block, an Error Amplifier block, a Current Limiter block, and a Thermal Protection block. The Shutdown Control block is connected to the  $\overline{\text{SHDN}}$  pin. The Voltage Reference block provides a reference voltage to the Error Amplifier. The Error Amplifier compares the reference voltage with the feedback voltage (taken from the output divider) and drives the MOSFET gate. The Current Limiter block limits the output current, and the Thermal Protection block monitors the junction temperature and shuts down the converter if it exceeds a threshold. A dashed box labeled with an asterisk (\*) encloses the Shutdown Control and the input diode, indicating that this configuration is only for 5-pin versions of the device.

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Input Voltage .....	+30V
Output Current (Continuous).....	$P_D / (V_{IN} - V_{OUT})$ mA
Output Current (Peak).....	300 mA
Output Voltage .....	$(V_{SS} - 0.3V)$ to $(V_{IN} + 0.3V)$
SHDN Voltage .....	$(V_{SS} - 0.3V)$ to +30V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Unless otherwise specified, all limits are established for  $V_{IN} = V_R + 2.0V$ , **Note 1**,  $C_{OUT} = 1 \mu F$  (X7R),  $C_{IN} = 1 \mu F$  (X7R),  $V_{SHDN} = V_{IN}$ ,  $T_A = +25^\circ C$

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Input / Output Characteristics</b>						
Input Operating Voltage	$V_{IN}$	2.0	—	28.0	V	<b>Note 1</b>
Input Quiescent Current	$I_Q$	—				$I_L = 0$ mA
		—	50	105	$\mu A$	$1.8V \leq V_{OUT} \leq 5.0V$
		—	60	115	$\mu A$	$5.1V \leq V_{OUT} \leq 12.0V$
		—	65	125	$\mu A$	$12.1V \leq V_{OUT} \leq 18.0V$
Shutdown Current	$I_{SHDN}$	—	0.01	0.10	$\mu A$	$SHDN = 0V$
Maximum Output Current	$I_{OUT}$	—				$V_{IN} = V_R + 3.0V$
		100	—	—	mA	$V_{OUT} < 3.0V$
		150	—	—	mA	$V_{OUT} \geq 3.0V$
Current Limiter	$I_{LIMIT}$	—	200	—	mA	
Output Short Circuit Current	$I_{OUT\_SC}$	—	40	—	mA	
Output Voltage Regulation	$V_{OUT}$	$V_R - 2.0\%$	$V_R$	$V_R + 2.0\%$	V	$I_{OUT} = 10$ mA, <b>Note 2</b>
$V_{OUT}$ Temperature Coefficient	$TCV_{OUT}$	—	$\pm 100$	—	ppm/ $^\circ C$	$I_{OUT} = 20$ mA, $-40^\circ C \leq T_A \leq +85^\circ C$ , <b>Note 3</b>

**Note 1:** The minimum  $V_{IN}$  must meet one condition:  $V_{IN} \geq (V_R + 2.0V)$ .

**2:**  $V_R$  is the nominal regulator output voltage with an input voltage of  $V_{IN} = V_R + 2.0V$ .

For example:  $V_R = 1.8V, 2.5V, 3.0V, 3.3V$ , etc.

**3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta Temperature)$ ,  $V_{OUT-HIGH}$  = highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .

**5:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of  $V_R + 2.0V$ .

# MCP1804

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all limits are established for $V_{IN} = V_R + 2.0V$ , <b>Note 1</b> , $C_{OUT} = 1 \mu F$ (X7R), $C_{IN} = 1 \mu F$ (X7R), $V_{SHDN} = V_{IN}$ , $T_A = +25^\circ C$						
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \cdot \Delta V_{IN})$	—				$(V_R + 2V) \leq V_{IN} \leq 28V$ , <b>Note 1</b>
		—	0.05	0.10	%/V	$I_{OUT} = 5 \text{ mA}$
		—	0.15	0.30	%/V	$I_{OUT} = 13 \text{ mA}$
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	—				$I_L = 1.0 \text{ mA to } 50 \text{ mA}$ , <b>Note 4</b>
		—	50	90	mV	$1.8V \leq V_{OUT} \leq 5.0V$
		—	110	175	mV	$5.1V \leq V_{OUT} \leq 12.0V$
		—	180	275	mV	$12.1V \leq V_{OUT} \leq 18.0V$
Dropout Voltage <b>Note 1, Note 5</b>	$V_{DROPOUT}$	—				$I_L = 20 \text{ mA}$
		—	550	710	mV	$1.8V \leq V_R \leq 1.9V$
		—	450	600	mV	$2.0V \leq V_R \leq 2.1V$
		—	390	520	mV	$2.2V \leq V_R \leq 2.4V$
		—	310	450	mV	$2.5V \leq V_R \leq 2.9V$
		—	260	360	mV	$3.0V \leq V_R \leq 3.9V$
		—	220	320	mV	$4.0V \leq V_R \leq 4.9V$
		—	190	280	mV	$5.0V \leq V_R \leq 6.4V$
		—	170	230	mV	$6.5V \leq V_R \leq 8.0V$
		—	130	190	mV	$8.1V \leq V_R \leq 10.0V$
		—	120	170	mV	$10.1V \leq V_R \leq 18.0V$
		—				$I_L = 100 \text{ mA}$
		—	2200	2700	mV	$1.8V \leq V_R \leq 1.9V$
		—	1900	2600	mV	$2.0V \leq V_R \leq 2.1V$
		—	1700	2200	mV	$2.2V \leq V_R \leq 2.4V$
		—	1500	1900	mV	$2.5V \leq V_R \leq 2.9V$
		—	1300	1700	mV	$3.0V \leq V_R \leq 3.9V$
		—	1100	1500	mV	$4.0V \leq V_R \leq 4.9V$
		—	1000	1300	mV	$5.0V \leq V_R \leq 6.4V$
		—	800	1150	mV	$6.5V \leq V_R \leq 8.0V$
		—	700	950	mV	$8.1V \leq V_R \leq 10.0V$
		—	650	850	mV	$10.1V \leq V_R \leq 18.0V$
SHDN "H" Voltage	$V_{SHDN\_H}$	1.1	—	$V_{IN}$	V	$V_{IN} = 28V$
SHDN "L" Voltage	$V_{SHDN\_L}$	0	—	0.35	V	$V_{IN} = 28V$
SHDN Current	$I_{SHDN}$	-0.1	—	0.1	$\mu A$	$V_{IN} = 28V$ , $V_{SHDN} = GND$ or $V_{IN}$

- Note 1:** The minimum  $V_{IN}$  must meet one condition:  $V_{IN} \geq (V_R + 2.0V)$ .
- 2:**  $V_R$  is the nominal regulator output voltage with an input voltage of  $V_{IN} = V_R + 2.0V$ .  
For example:  $V_R = 1.8V, 2.5V, 3.0V, 3.3V$ , etc.
- 3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) \cdot 10^6 / (V_R \cdot \Delta \text{Temperature})$ ,  $V_{OUT-HIGH}$  = highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = lowest voltage measured over the temperature range.
- 4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .
- 5:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of  $V_R + 2.0V$ .

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Specifications:** Unless otherwise specified, all limits are established for  $V_{IN} = V_R + 2.0V$ , **Note 1**,  $C_{OUT} = 1 \mu F$  (X7R),  $C_{IN} = 1 \mu F$  (X7R),  $V_{SHDN} = V_{IN}$ ,  $T_A = +25^\circ C$

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Ripple Rejection Ratio	PSRR	—	50	—	dB	$f = 1 \text{ kHz}$ , $I_L = 20 \text{ mA}$ , $V_{IN\_AC} = 0.5V \text{ pk-pk}$ , $C_{IN} = 0 \mu F$
Thermal Shutdown Protection	TSD	—	150	—	$^\circ C$	$T_J = 150^\circ C$
Thermal Shutdown Hysteresis	$\Delta TSD$	—	25	—	$^\circ C$	

**Note 1:** The minimum  $V_{IN}$  must meet one condition:  $V_{IN} \geq (V_R + 2.0V)$ .

**2:**  $V_R$  is the nominal regulator output voltage with an input voltage of  $V_{IN} = V_R + 2.0V$ .  
For example:  $V_R = 1.8V, 2.5V, 3.0V, 3.3V$ , etc.

**3:**  $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) * 10^6 / (V_R * \Delta \text{Temperature})$ ,  $V_{OUT-HIGH}$  = highest voltage measured over the temperature range.  $V_{OUT-LOW}$  = lowest voltage measured over the temperature range.

**4:** Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Changes in output voltage due to heating effects are determined using thermal regulation specification  $TCV_{OUT}$ .

**5:** Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its measured value with an applied input voltage of  $V_R + 2.0V$ .

**TEMPERATURE SPECIFICATIONS**

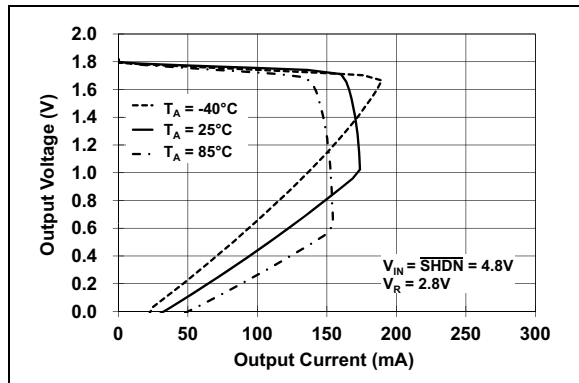
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+85	$^\circ C$	
Operating Junction Temperature Range	$T_J$	-40	—	+125	$^\circ C$	
Storage Temperature Range	$T_A$	-55	—	+125	$^\circ C$	
<b>Thermal Package Resistance</b>						
Thermal Resistance, 3LD SOT-89	$\theta_{JA}$	—	180	—	$^\circ C/W$	EIA/JEDEC® JESD51-7 FR-4 0.063 4-Layer Board
	$\theta_{JC}$	—	52	—		
Thermal Resistance, 3LD SOT-223	$\theta_{JA}$	—	62	—	$^\circ C/W$	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board
	$\theta_{JC}$	—	15	—		
Thermal Resistance, 5LD SOT-23	$\theta_{JA}$	—	256	—	$^\circ C/W$	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board
	$\theta_{JC}$	—	81	—		
Thermal Resistance, 5LD SOT-89	$\theta_{JA}$	—	180	—	$^\circ C/W$	EIA/JEDEC JESD51-7 FR-4 0.063 4-Layer Board
	$\theta_{JC}$	—	52	—		

# MCP1804

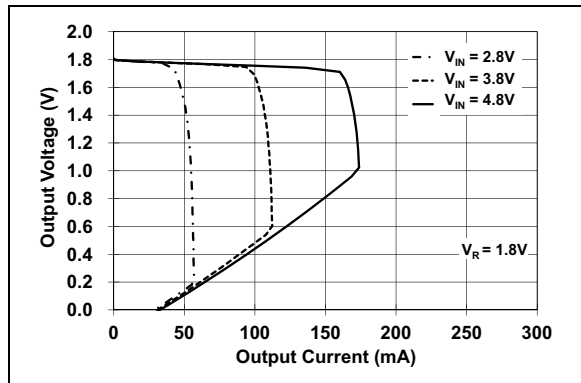
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

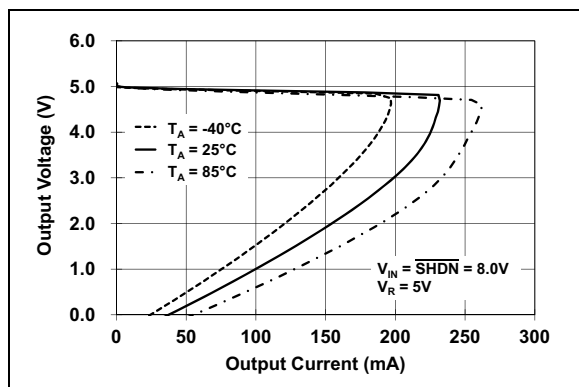
**Note:** Unless otherwise indicated:  $C_{OUT} = 1 \mu F$  Ceramic (X7R),  $C_{IN} = 1 \mu F$  Ceramic (X7R),  $T_A = +25^\circ C$ ,  $V_{IN} = V_R + 2.0V$ .



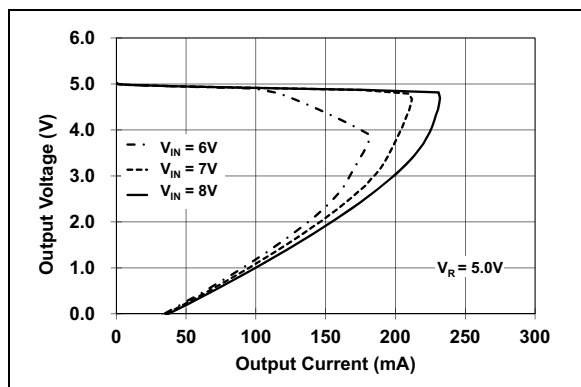
**FIGURE 2-1:** Output Voltage vs. Output Current.



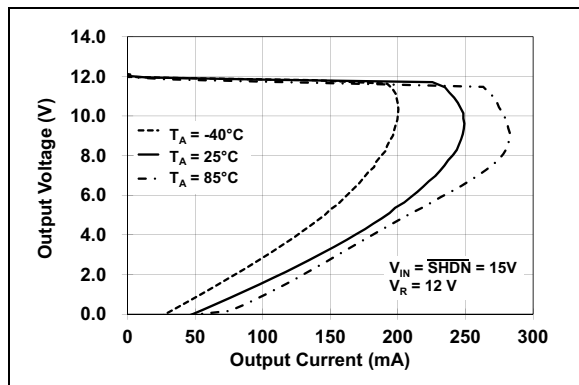
**FIGURE 2-4:** Output Voltage vs. Output Current.



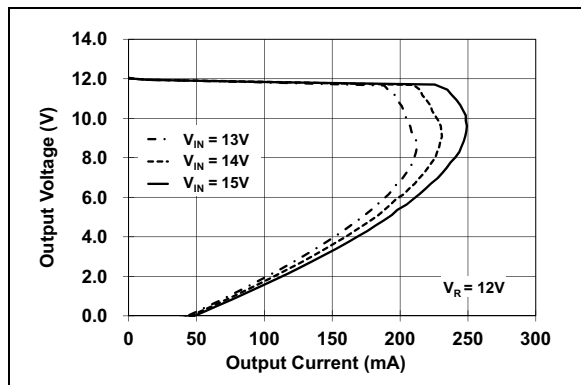
**FIGURE 2-2:** Output Voltage vs. Output Current.



**FIGURE 2-5:** Output Voltage vs. Output Current.

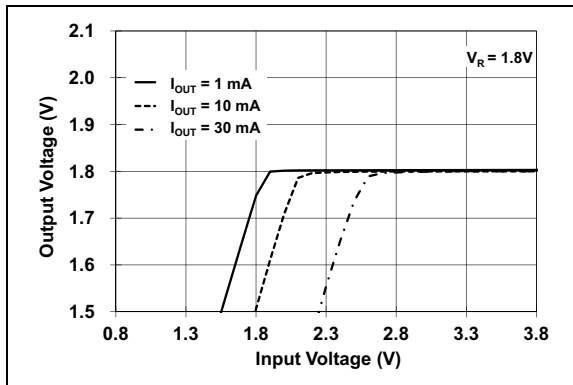


**FIGURE 2-3:** Output Voltage vs. Output Current.

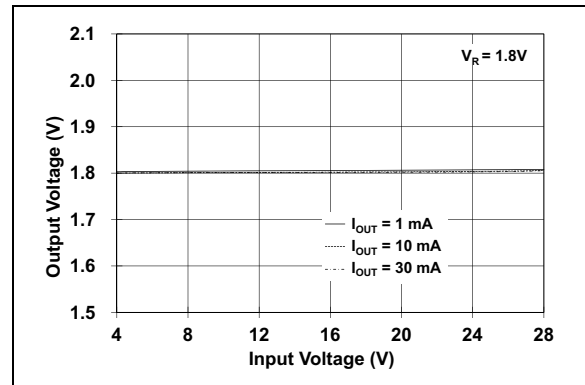


**FIGURE 2-6:** Output Voltage vs. Output Current.

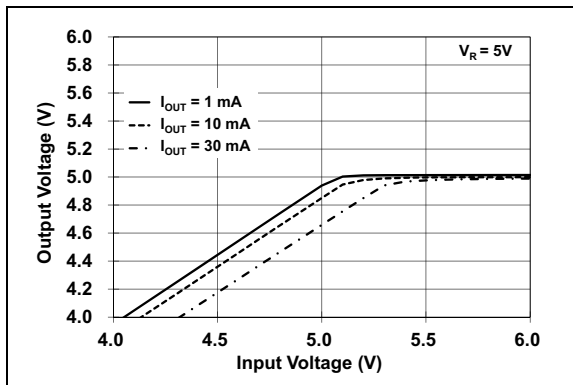
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



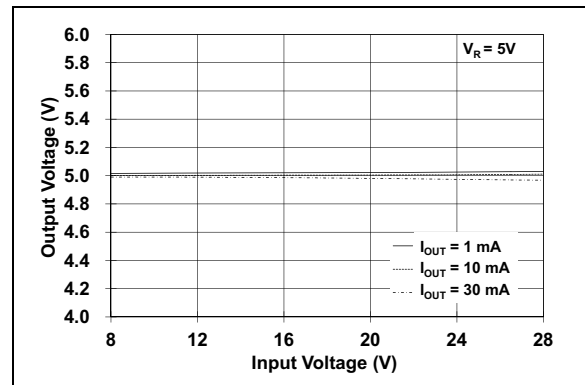
**FIGURE 2-7:** Output Voltage vs. Input Voltage.



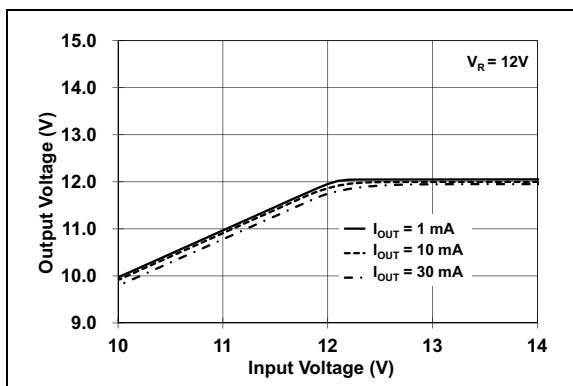
**FIGURE 2-10:** Output Voltage vs. Input Voltage.



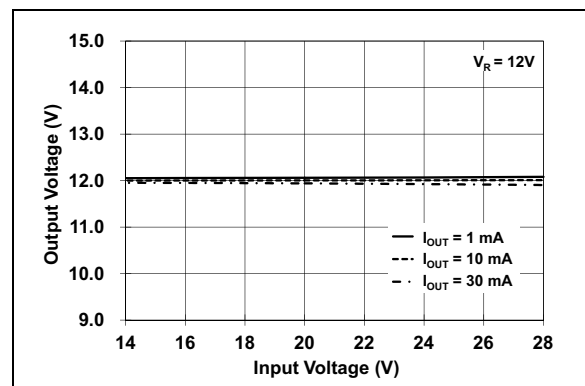
**FIGURE 2-8:** Output Voltage vs. Input Voltage.



**FIGURE 2-11:** Output Voltage vs. Input Voltage.



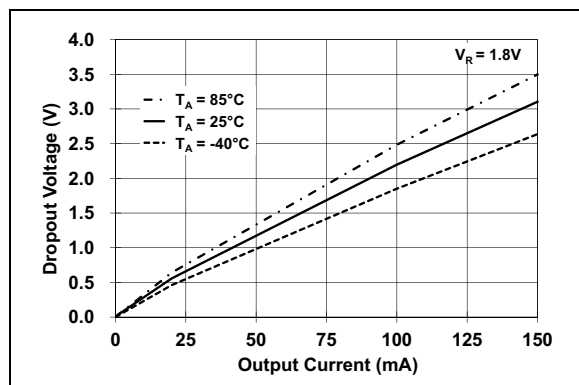
**FIGURE 2-9:** Output Voltage vs. Input Voltage.



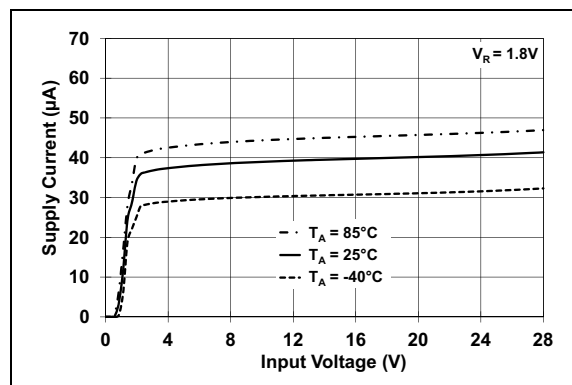
**FIGURE 2-12:** Output Voltage vs. Input Voltage.

# MCP1804

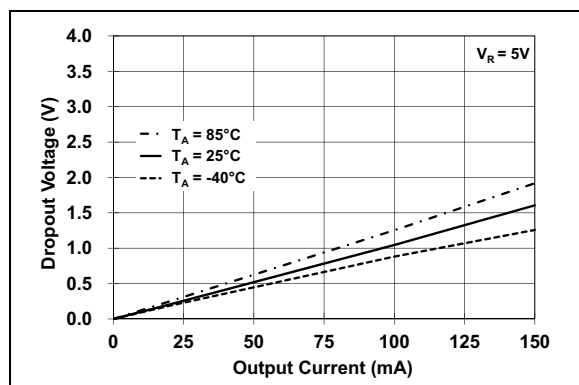
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



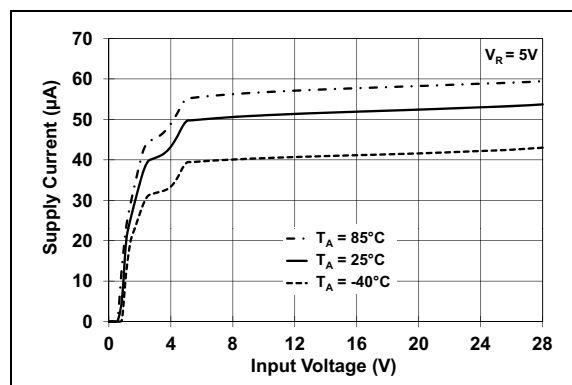
**FIGURE 2-13:** Dropout Voltage vs. Load Current.



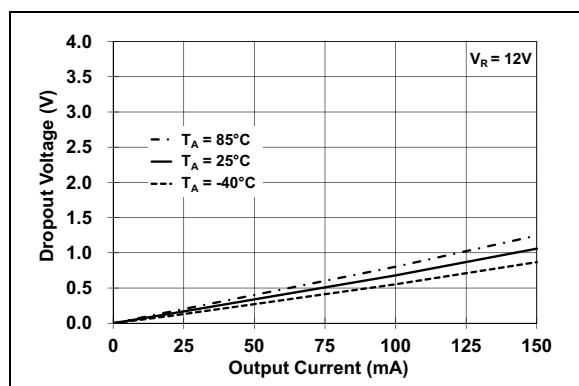
**FIGURE 2-16:** Supply Current vs. Input Voltage.



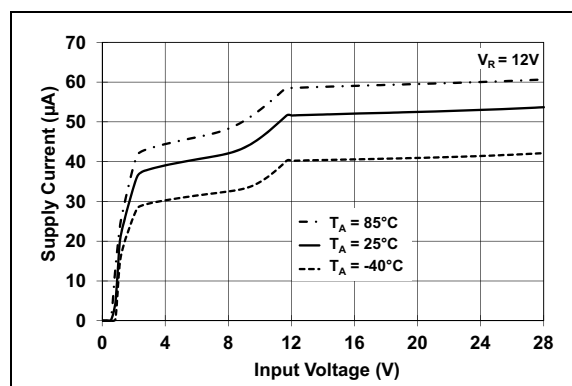
**FIGURE 2-14:** Dropout Voltage vs. Load Current.



**FIGURE 2-17:** Supply Current vs. Input Voltage.



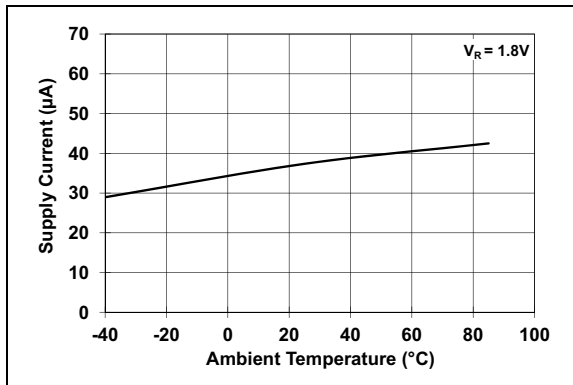
**FIGURE 2-15:** Dropout Voltage vs. Load Current.



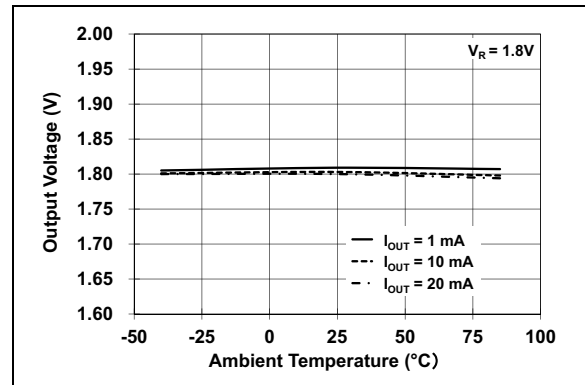
**FIGURE 2-18:** Supply Current vs. Input Voltage.



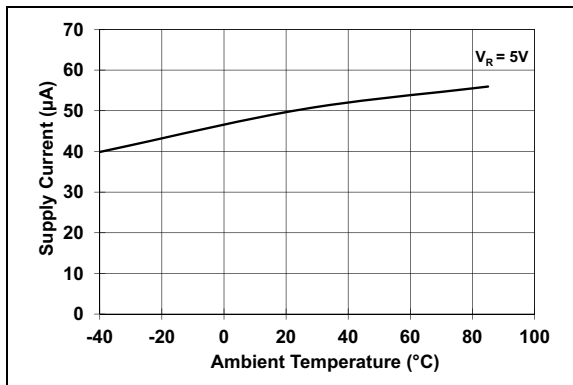
**Note:** Unless otherwise indicated:  $C_{OUT} = 1 \mu F$  Ceramic (X7R),  $C_{IN} = 1 \mu F$  Ceramic (X7R),  $T_A = +25^\circ C$ ,  $V_{IN} = V_R + 2.0V$ .



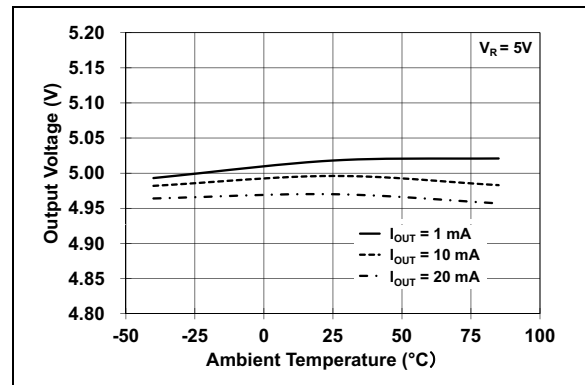
**FIGURE 2-19:** Supply Current vs. Input Voltage.



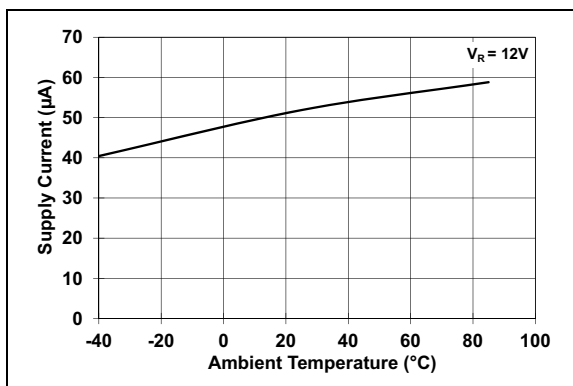
**FIGURE 2-22:** Output Voltage vs. Ambient Temperature.



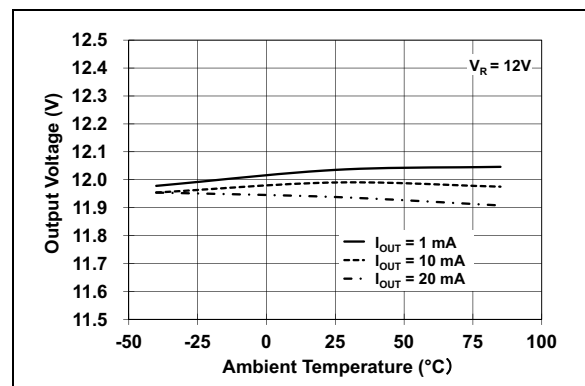
**FIGURE 2-20:** Supply Current vs. Input Voltage.



**FIGURE 2-23:** Output Voltage vs. Ambient Temperature.



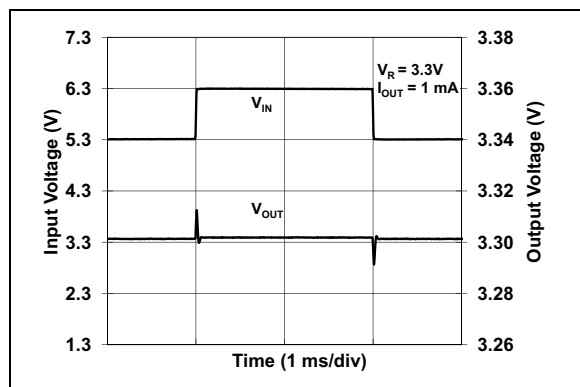
**FIGURE 2-21:** Supply Current vs. Input Voltage.



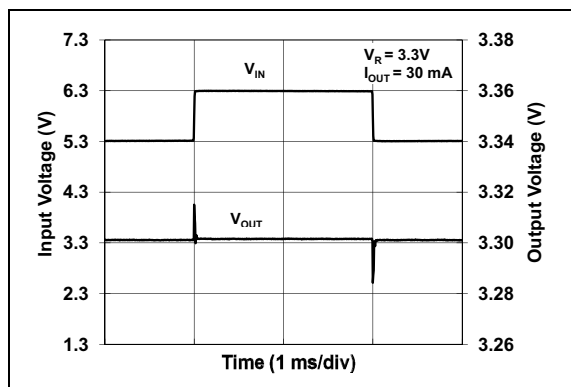
**FIGURE 2-24:** Output Voltage vs. Ambient Temperature.

# MCP1804

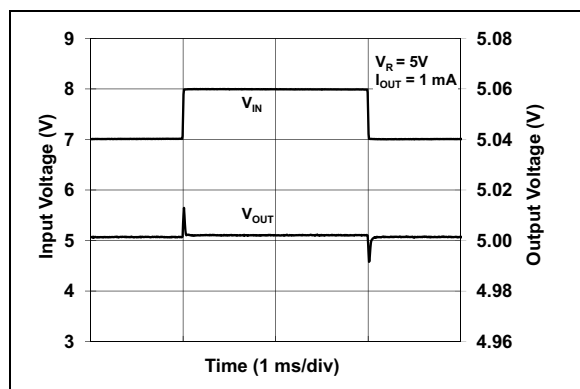
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



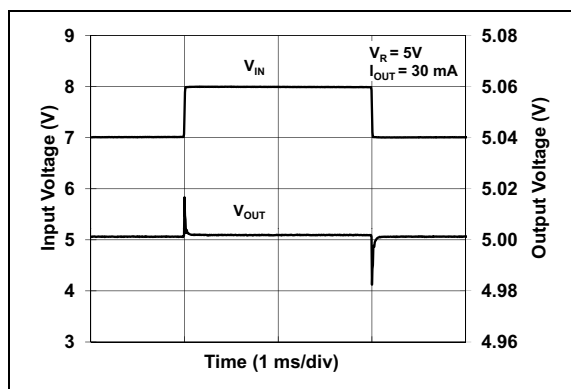
**FIGURE 2-25:** Dynamic Line Response.



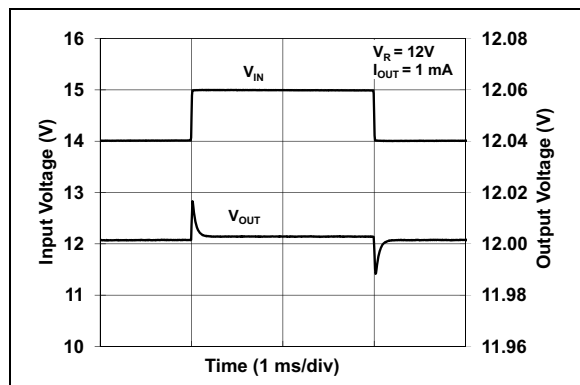
**FIGURE 2-28:** Dynamic Line Response.



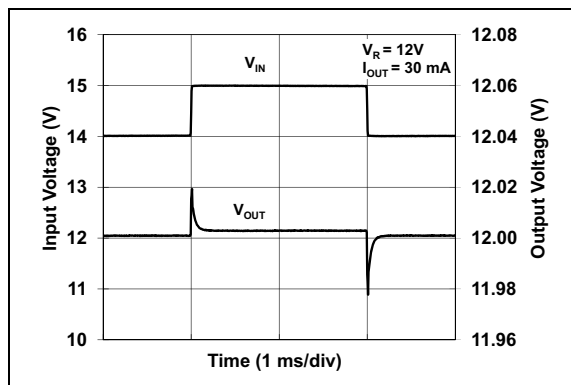
**FIGURE 2-26:** Dynamic Line Response.



**FIGURE 2-29:** Dynamic Line Response.

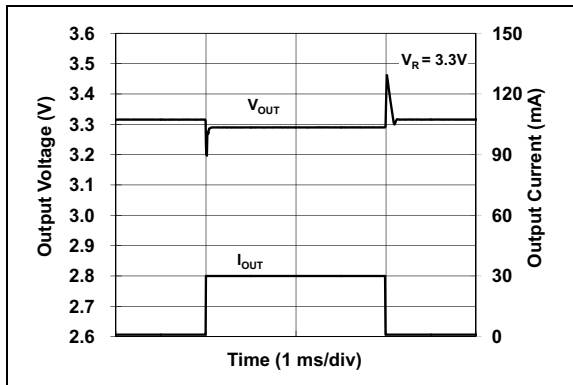


**FIGURE 2-27:** Dynamic Line Response.

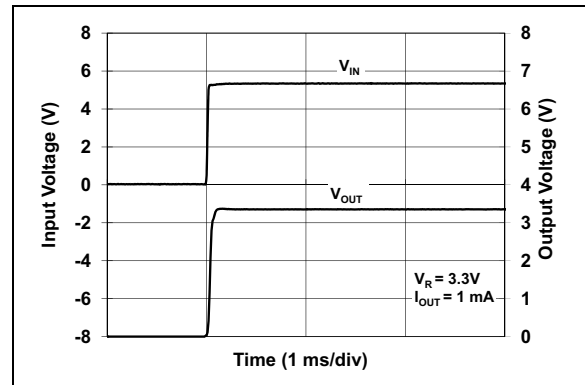


**FIGURE 2-30:** Dynamic Line Response.

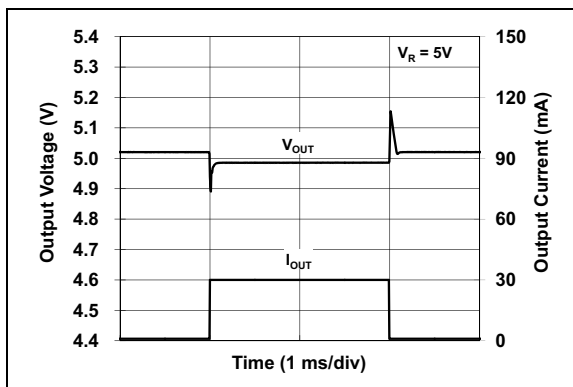
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



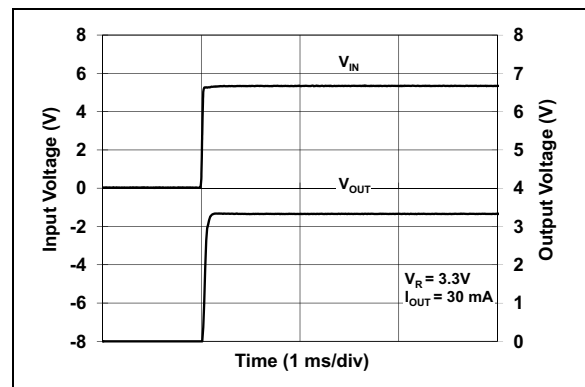
**FIGURE 2-31:** Dynamic Load Response.



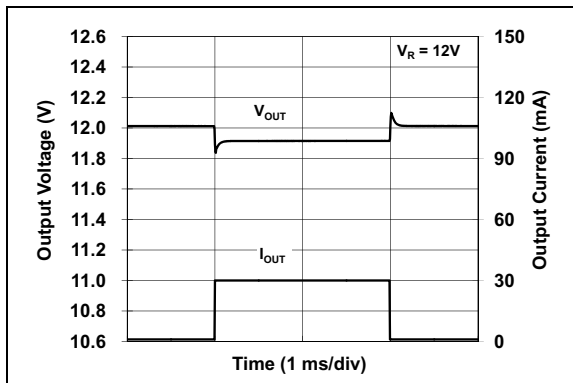
**FIGURE 2-34:** Start-up Response.



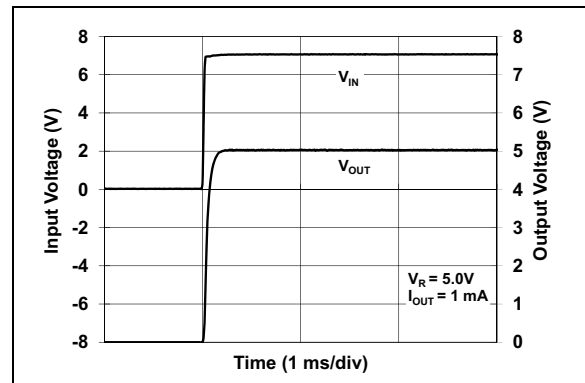
**FIGURE 2-32:** Dynamic Load Response.



**FIGURE 2-35:** Start-up Response.



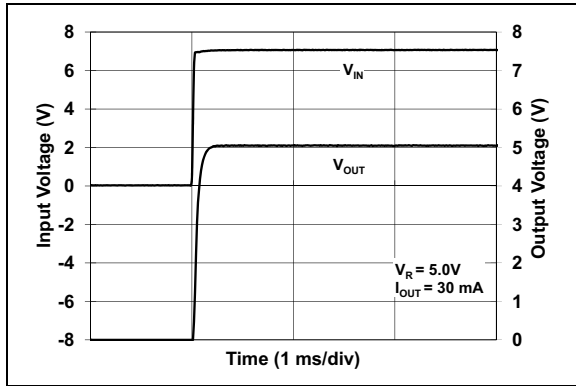
**FIGURE 2-33:** Dynamic Load Response.



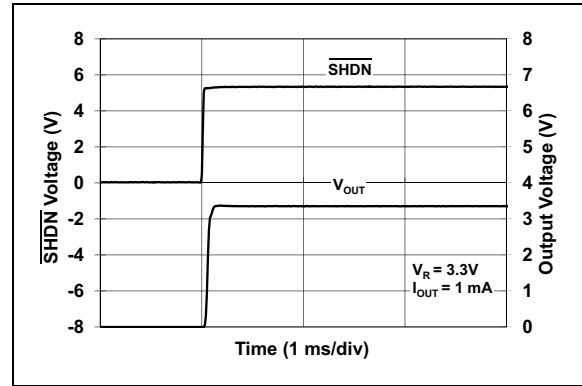
**FIGURE 2-36:** Start-up Response.

# MCP1804

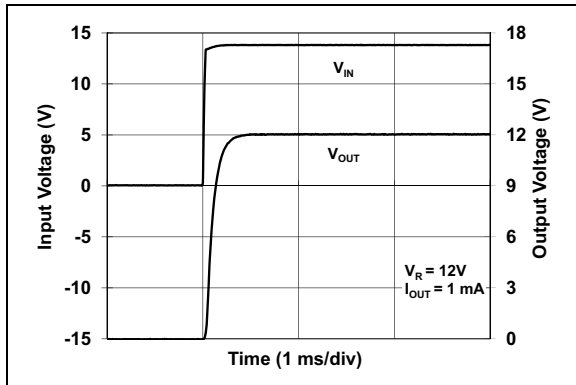
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



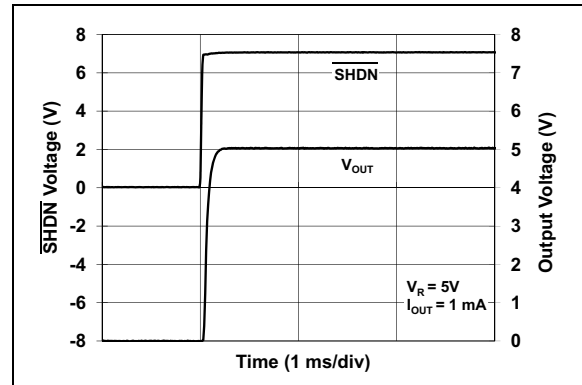
**FIGURE 2-37:** Start-up Response.



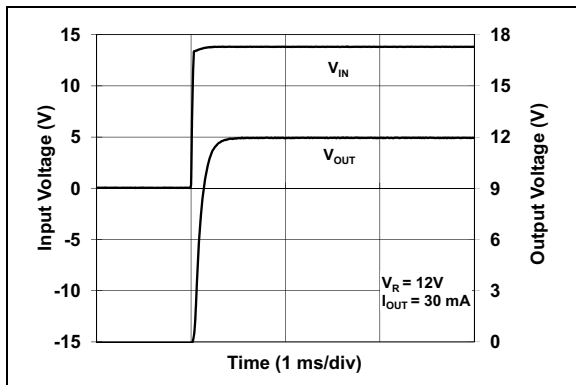
**FIGURE 2-40:** SHDN Response.



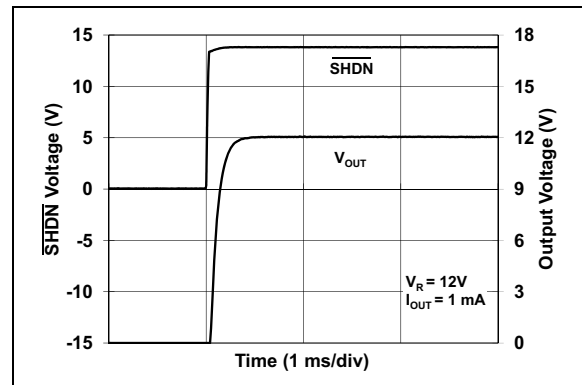
**FIGURE 2-38:** Start-up Response.



**FIGURE 2-41:** SHDN Response.

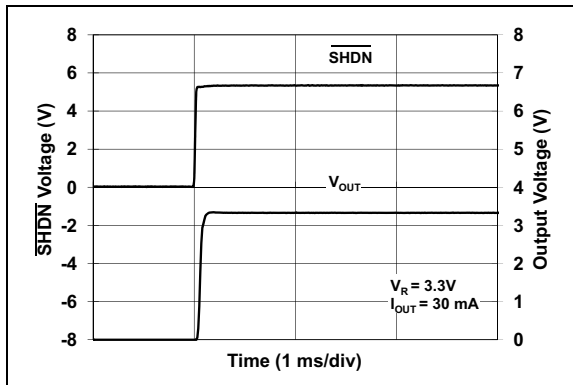


**FIGURE 2-39:** Start-up Response.

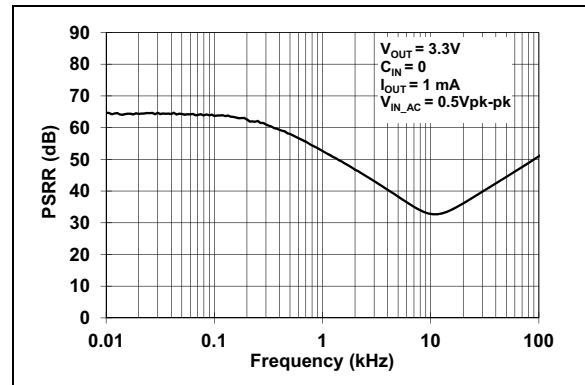


**FIGURE 2-42:** SHDN Response.

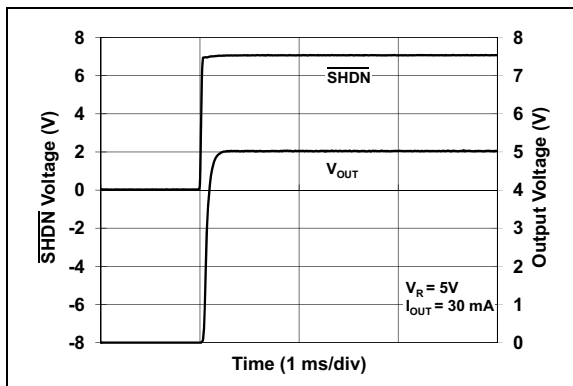
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



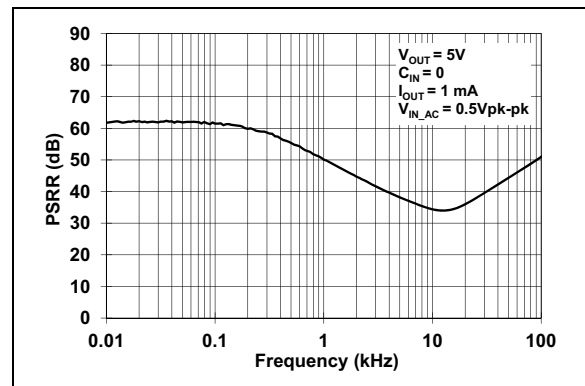
**FIGURE 2-43:** SHDN Response.



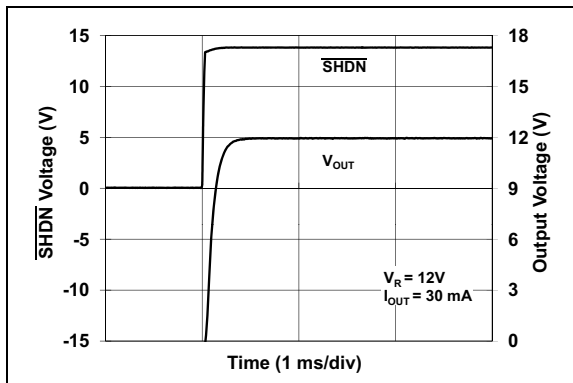
**FIGURE 2-46:** PSRR 3.3V @ 1 mA.



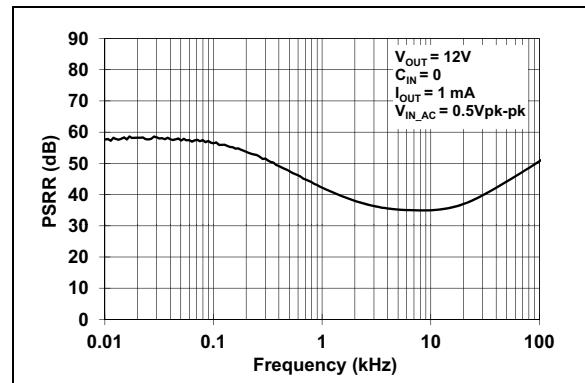
**FIGURE 2-44:** SHDN Response.



**FIGURE 2-47:** PSRR 5.0V @ 1 mA.



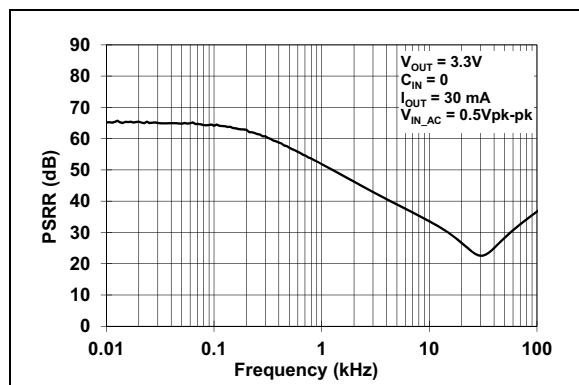
**FIGURE 2-45:** SHDN Response.



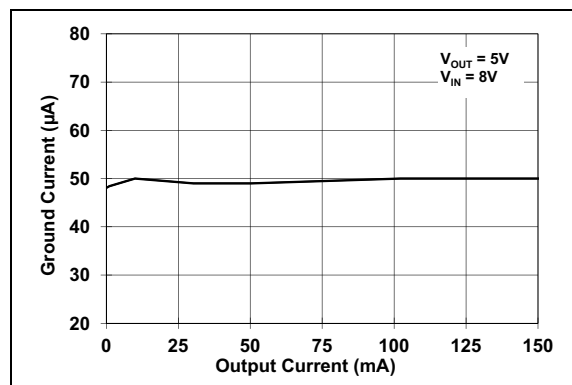
**FIGURE 2-48:** PSRR 12.0V @ 1 mA.

# MCP1804

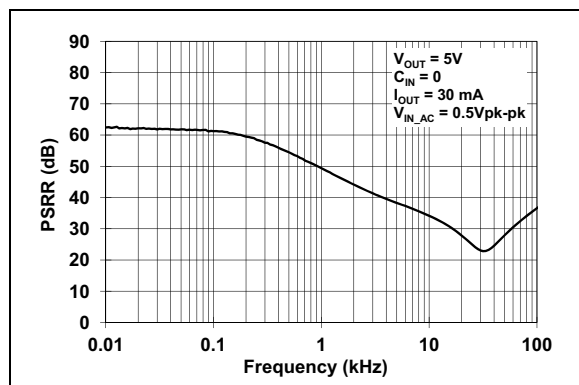
**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



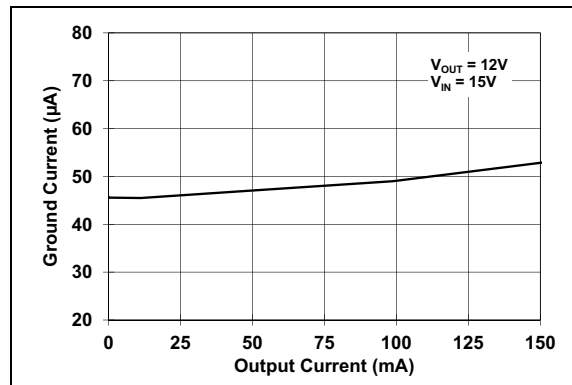
**FIGURE 2-49:** PSRR 3.3V @ 30 mA.



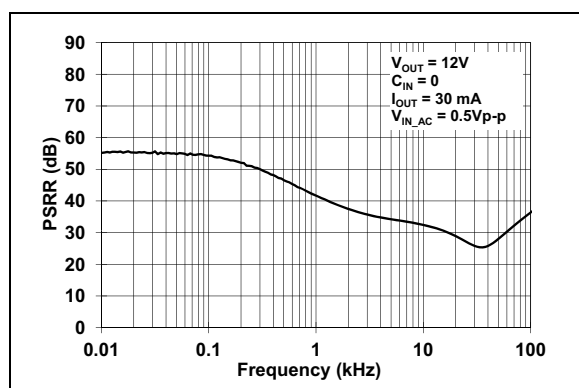
**FIGURE 2-52:** Ground Current vs. Output Current.



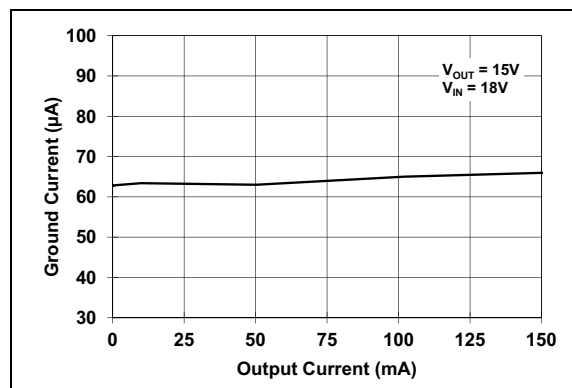
**FIGURE 2-50:** PSRR 5.0V @ 30 mA.



**FIGURE 2-53:** Ground Current vs. Output Current.

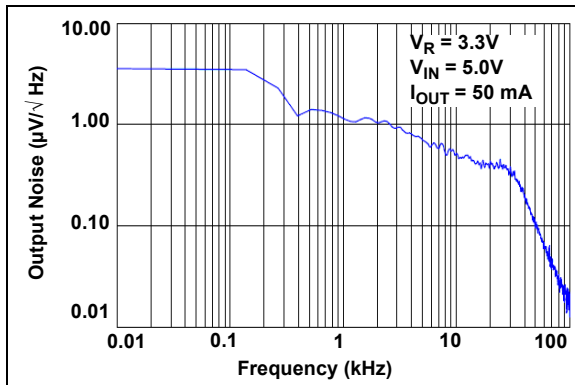


**FIGURE 2-51:** PSRR 12V @ 30 mA.



**FIGURE 2-54:** Ground Current vs. Output Current.

**Note:** Unless otherwise indicated:  $C_{OUT} = 1\ \mu\text{F}$  Ceramic (X7R),  $C_{IN} = 1\ \mu\text{F}$  Ceramic (X7R),  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = V_R + 2.0\text{V}$ .



**FIGURE 2-55:** Output Noise vs. Frequency.

# MCP1804

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: MCP1804 PIN FUNCTION TABLE**

MCP1804				Symbol	Description
SOT-23-5	SOT-89-5	SOT-89-3	SOT-223-3		
1	5	3	3	$V_{IN}$	Unregulated Supply Voltage
2	2, TAB	2, TAB	2, TAB	GND	Ground Terminal
3	4	—	—	NC	No connection
4	3	—	—	$\overline{\text{SHDN}}$	Shutdown
5	1	1	1	$V_{OUT}$	Regulated Voltage Output

### 3.1 Unregulated Input Voltage ( $V_{IN}$ )

Connect  $V_{IN}$  to the input unregulated source voltage. Like all low dropout linear regulators, low source impedance is necessary for the stable operation of the LDO. The amount of capacitance required to ensure low source impedance will depend on the proximity of the input source capacitors or battery type. For most applications, 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  of capacitance will ensure stable operation of the LDO circuit. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

### 3.2 Ground Terminal (GND)

Regulator ground. Tie GND to the negative side of the output and the negative side of the input capacitor. Only the LDO bias current (50 to 60  $\mu\text{A}$  typical) flows out of this pin; there is no high current. The LDO output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

### 3.3 Shutdown Input ( $\overline{\text{SHDN}}$ )

The  $\overline{\text{SHDN}}$  input is used to turn the LDO output voltage on and off. When the  $\overline{\text{SHDN}}$  input is at a logic-high level, the LDO output voltage is enabled. When the  $\overline{\text{SHDN}}$  input is pulled to a logic-low level, the LDO output voltage is disabled and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.01  $\mu\text{A}$ . The  $\overline{\text{SHDN}}$  pin does not have an internal pull-up or pull-down resistor. The  $\overline{\text{SHDN}}$  pin must be connected to either  $V_{IN}$  or GND to prevent the device from becoming unstable.

### 3.4 Regulated Output Voltage ( $V_{OUT}$ )

Connect  $V_{OUT}$  to the positive side of the load and the positive terminal of the output capacitor. The positive side of the output capacitor should be physically located as close to the LDO  $V_{OUT}$  pin as is practical. The current flowing out of this pin is equal to the DC load current. For most applications, 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  of capacitance will ensure stable operation of the LDO circuit. Larger values may be used to improve dynamic load response. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

### 3.5 No Connect (NC)

No internal connection. The pins marked NC are true “No Connect” pins.



## 4.0 DETAILED DESCRIPTION

### 4.1 Output Regulation

A portion of the LDO output voltage is fed back to the internal error amplifier and compared with the precision internal bandgap reference. The error amplifier output will adjust the amount of current that flows through the P-Channel pass transistor, thus regulating the output voltage to the desired value. Any changes in input voltage or output current will cause the error amplifier to respond and adjust the output voltage to the target voltage (refer to [Figure 4-1](#)).

### 4.2 Overcurrent

The MCP1804 internal circuitry monitors the amount of current flowing through the P-Channel pass transistor. In the event that the load current reaches the current limiter level of 200 mA (typical), the current limiter circuit will operate and the output voltage will drop. As the output voltage drops, the internal current foldback circuit will further reduce the output voltage causing the output current to decrease. When the output is shorted, a typical output current of 50 mA flows.

### 4.3 Shutdown

The  $\overline{\text{SHDN}}$  input is used to turn the LDO output voltage on and off. When the  $\overline{\text{SHDN}}$  input is at a logic-high level, the LDO output voltage is enabled. When the  $\overline{\text{SHDN}}$  input is pulled to a logic-low level, the LDO output voltage is disabled and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.01  $\mu\text{A}$ . The  $\overline{\text{SHDN}}$  pin does not have an internal pull-up or pull-down resistor. Therefore the  $\overline{\text{SHDN}}$  pin must be pulled either high or low to prevent the device from becoming unstable. The internal device current will increase when the device is operational and current flows through the pull-up or pull-down resistor to the  $\overline{\text{SHDN}}$  pin internal logic. The  $\overline{\text{SHDN}}$  pin internal logic is equivalent to an inverter input.

### 4.4 Output Capacitor

The MCP1804 requires a minimum output capacitance of 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients.

Larger LDO output capacitors can be used with the MCP1804 to improve dynamic performance and power supply ripple rejection performance. Aluminum-electrolytic capacitors are not recommended for low temperature applications of  $< -25^{\circ}\text{C}$ .

### 4.5 Input Capacitor

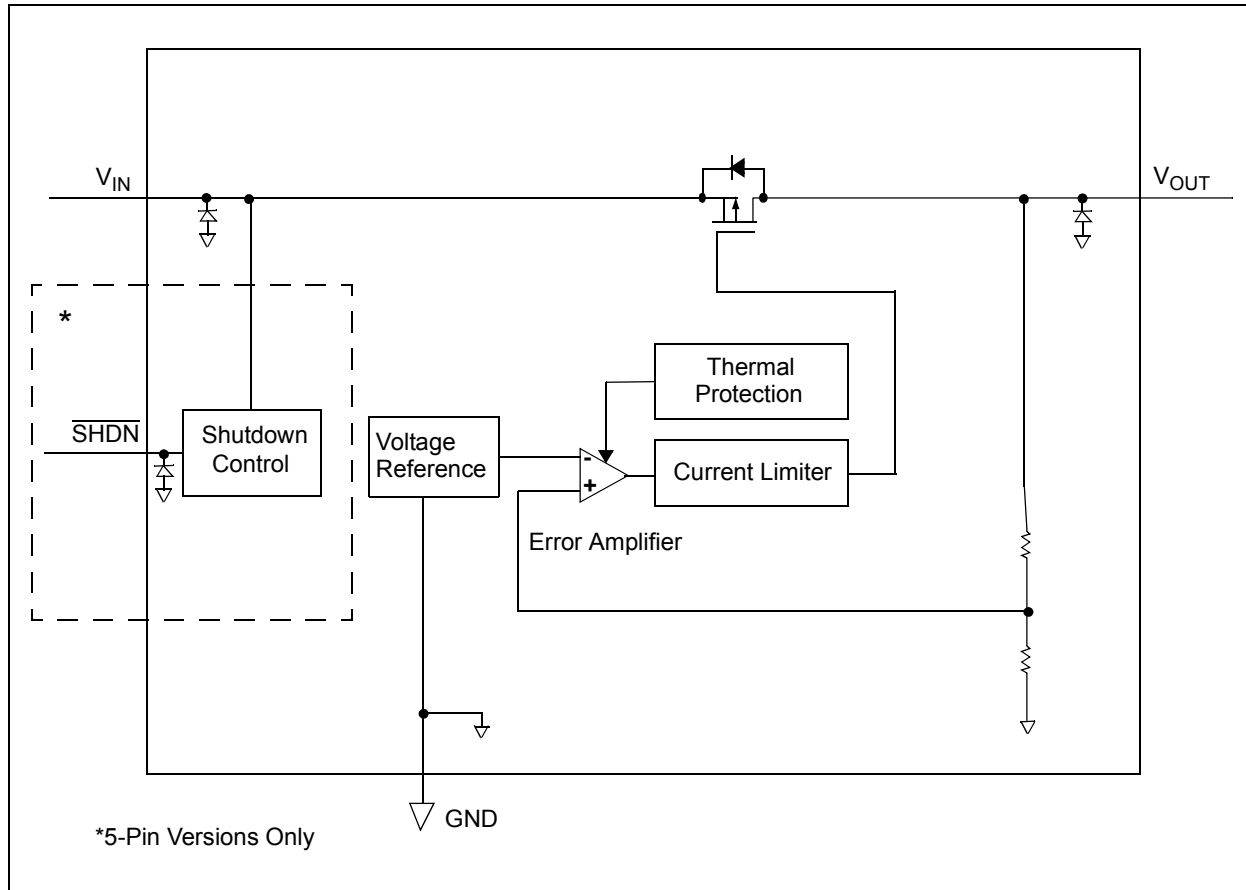
Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries or in applications with long lead length ( $> 10$  inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent or higher value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

### 4.6 Thermal Shutdown

The MCP1804 thermal shutdown circuitry protects the device when the internal junction temperature reaches the typical thermal limit value of  $+150^{\circ}\text{C}$ . The thermal limit shuts off the output drive transistor. Device output will resume when the internal junction temperature falls below the thermal limit value by an amount equal to the thermal limit hysteresis value of  $+25^{\circ}\text{C}$ .

# MCP1804



**FIGURE 4-1:** Block Diagram.

## 5.0 FUNCTIONAL DESCRIPTION

The MCP1804 CMOS linear regulator is intended for applications that need low current consumption while maintaining output voltage regulation. The operating continuous load of the MCP1804 ranges from 0 mA to 150 mA. The input operating voltage ranges from 2.0V to 28.0V, making it capable of operating from a single 12V battery or single and multiple Li-Ion cell batteries.

### 5.1 Input

The input of the MCP1804 is connected to the source of the P-Channel PMOS pass transistor. As with all LDO circuits, a relatively low source impedance ( $< 10\Omega$ ) is needed to prevent the input impedance from causing the LDO to become unstable. The size and type of the capacitor needed depend heavily on the input source type (battery, power supply) and the output current range of the application. For most applications, a 0.1  $\mu\text{F}$  ceramic capacitor will be sufficient to ensure circuit stability. Larger values can be used to improve circuit AC performance.

### 5.2 Output

The maximum rated continuous output current for the MCP1804 is 150 mA.

A minimum output capacitance of 0.1  $\mu\text{F}$  to 1.0  $\mu\text{F}$  is required for small signal stability in applications that have up to 150 mA output current capability. The capacitor type can be ceramic, tantalum or aluminum electrolytic.

# MCP1804

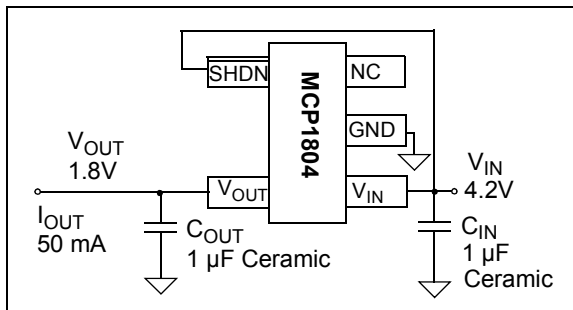
---

NOTES:

## 6.0 APPLICATION CIRCUITS AND ISSUES

### 6.1 Typical Application

The MCP1804 is most commonly used as a voltage regulator. Its low quiescent current and wide input voltage make it ideal for Li-Ion and 12V battery-powered applications.



**FIGURE 6-1:** Typical Application Circuit.

#### 6.1.1 APPLICATION INPUT CONDITIONS

Package Type	= SOT-23
Input Voltage Range	= 3.8V to 4.2V
V <sub>IN</sub> maximum	= 4.6V
V <sub>OUT</sub> typical	= 1.8V
I <sub>OUT</sub>	= 50 mA maximum

## 6.2 Power Calculations

### 6.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1804 is a function of input voltage, output voltage and output current. The power dissipation resulting from the quiescent current draw is so low it is insignificant (50.0 µA × V<sub>IN</sub>). The following equation can be used to calculate the internal power dissipation of the LDO.

#### EQUATION 6-1:

$$P_{LDO} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT}$$

Where:

P <sub>LDO</sub>	= Internal power dissipation of the LDO Pass device
V <sub>IN(MAX)</sub>	= Maximum input voltage
V <sub>OUT(MIN)</sub>	= Minimum output voltage of the LDO

The maximum continuous operating temperature specified for the MCP1804 is +85°C. To estimate the internal junction temperature of the MCP1804, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient (R<sub>θJA</sub>). The thermal resistance from junction to ambient for the SOT-23 pin package is estimated at 256°C/W.

#### EQUATION 6-2:

$$T_{J(MAX)} = P_{TOTAL} \times R_{\theta JA} + T_{A(MAX)}$$

Where:

T <sub>J(MAX)</sub>	= Maximum continuous junction temperature
P <sub>TOTAL</sub>	= Total power dissipation of the device
R <sub>θJA</sub>	= Thermal resistance from junction to ambient
T <sub>A(MAX)</sub>	= Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

#### EQUATION 6-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R_{\theta JA}}$$

Where:

P <sub>D(MAX)</sub>	= Maximum power dissipation of the device
T <sub>J(MAX)</sub>	= Maximum continuous junction temperature
T <sub>A(MAX)</sub>	= Maximum ambient temperature
R <sub>θJA</sub>	= Thermal resistance from junction to ambient

#### EQUATION 6-4:

$$T_{J(RISE)} = P_{D(MAX)} \times R_{\theta JA}$$

Where:

T <sub>J(RISE)</sub>	= Rise in the device's junction temperature over the ambient temperature
P <sub>D(MAX)</sub>	= Maximum power dissipation of the device
R <sub>θJA</sub>	= Thermal resistance from junction to ambient

#### EQUATION 6-5:

$$T_J = T_{J(RISE)} + T_A$$

Where:

T <sub>J</sub>	= Junction Temperature
T <sub>J(RISE)</sub>	= Rise in the device's junction temperature over the ambient temperature
T <sub>A</sub>	= Ambient temperature

# MCP1804

## 6.3 Voltage Regulator

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation resulting from ground current is small enough to be neglected.

### 6.3.1 POWER DISSIPATION EXAMPLE

<b>Package:</b>	
Package Type =	SOT-23
<b>Input Voltage:</b>	
$V_{IN}$ =	3.8V to 4.6V
<b>LDO Output Voltages and Currents:</b>	
$V_{OUT}$ =	1.8V
$I_{OUT}$ =	50 mA
<b>Maximum Ambient Temperature:</b>	
$T_{A(MAX)}$ =	+40°C
<b>Internal Power Dissipation:</b>	
Internal Power dissipation is the product of the LDO output current times the voltage across the LDO ( $V_{IN}$ to $V_{OUT}$ ).	
$P_{LDO(MAX)}$ =	$(V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$
$P_{LDO(MAX)}$ =	$(4.6V - (0.98 \times 1.8V)) \times 50 \text{ mA}$
$P_{LDO(MAX)}$ =	141.8 milli-Watts

#### 6.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ( $R_{\theta JA}$ ) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, "High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages". The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, "A Method to Determine How Much Power a SOT23 Can Dissipate in an Application" (DS00792), for more information regarding this subject.

$$T_{J(RISE)} = P_{TOTAL} \times R_{\theta JA}$$

$$T_{J(RISE)} = 141.8 \text{ milli-Watts} \times 256.0^\circ\text{C/Watt}$$

$$T_{J(RISE)} = 36.3^\circ\text{C}$$

#### 6.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$$T_J = T_{J(RISE)} + T_{A(MAX)}$$

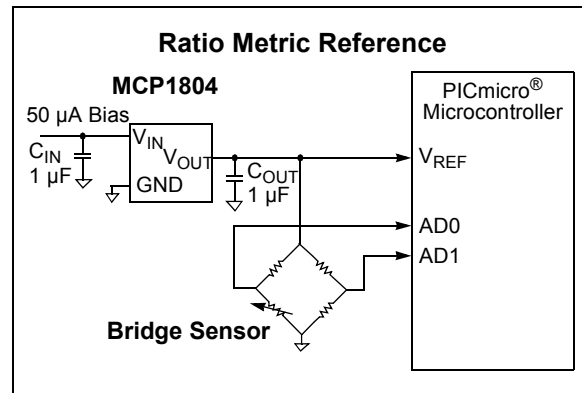
$$T_J = 76.3^\circ\text{C}$$

### Maximum Package Power Dissipation at +25°C Ambient Temperature (minimum PCB footprint)

SOT-23 (256°C/Watt = $R_{\theta JA}$ ):	
$P_{D(MAX)}$ =	$(125^\circ\text{C} - 25^\circ\text{C}) / 256^\circ\text{C/W}$
$P_{D(MAX)}$ =	390 milli-Watts
SOT-89 (180°C/Watt = $R_{\theta JA}$ ):	
$P_{D(MAX)}$ =	$(125^\circ\text{C} - 25^\circ\text{C}) / 180^\circ\text{C/W}$
$P_{D(MAX)}$ =	555 milli-Watts

## 6.4 Voltage Reference

The MCP1804 can be used not only as a regulator, but also as a low quiescent current voltage reference. In many microcontroller applications, the initial accuracy of the reference can be calibrated using production test equipment or by using a ratio measurement. When the initial accuracy is calibrated, the thermal stability and line regulation tolerance are the only errors introduced by the MCP1804 LDO. The low-cost, low quiescent current and small ceramic output capacitor are all advantages when using the MCP1804 as a voltage reference.



**FIGURE 6-2:** Using the MCP1804 as a Voltage Reference.

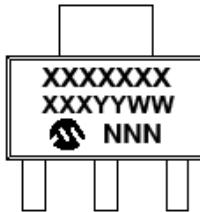
## 6.5 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 150 mA maximum specification of the MCP1804. The internal current limit of the MCP1804 will prevent high peak load demands from causing non-recoverable damage. The 150 mA rating is a maximum average continuous rating. As long as the average current does not exceed 150 mA or the maximum power dissipation of the packaged device, pulsed higher load currents can be applied to the MCP1804. The typical current limit for the MCP1804 is 200 mA ( $T_A = +25^\circ\text{C}$ ).

## 7.0 PACKAGING INFORMATION

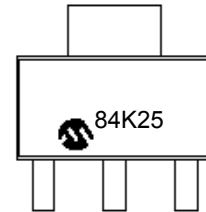
### 7.1 Package Marking Information

3-Lead SOT-223

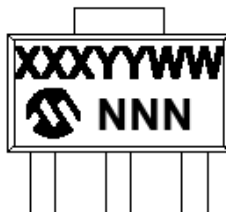


Part Number	Code
MCP1804T-1802I/DB	84KXX
MCP1804T-2502I/DB	84TXX
MCP1804T-3002I/DB	84ZXX
MCP1804T-3302I/DB	852XX
MCP1804T-5002I/DB	85MXX
MCP1804T-A002I/DB	879XX
MCP1804T-C002I/DB	87ZXX

Example

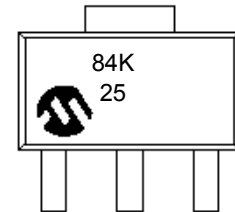


3-Lead SOT-89

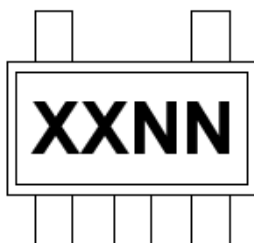


Part Number	Code
MCP1804T-1802I/MB	84KXX
MCP1804T-2502I/MB	84TXX
MCP1804T-3002I/MB	84ZXX
MCP1804T-3302I/MB	852XX
MCP1804T-5002I/MB	85MXX
MCP1804T-A002I/MB	879XX
MCP1804T-C002I/MB	87ZXX

Example

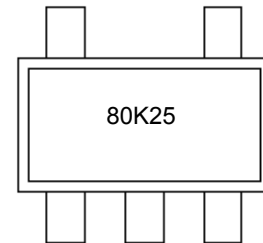


5-Lead SOT-23



Part Number	Code
MCP1804T-1802I/OT	80KXX
MCP1804T-2502I/OT	80TXX
MCP1804T-3002I/OT	80ZXX
MCP1804T-3302I/OT	812XX
MCP1804T-5002I/OT	81MXX
MCP1804T-A002I/OT	839XX
MCP1804T-C002I/OT	83ZXX

Example

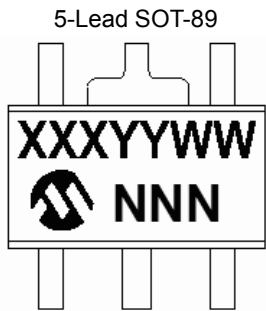


**Legend:** XX...X Customer-specific information  
Y Year code (last digit of calendar year)  
YY Year code (last 2 digits of calendar year)  
WW Week code (week of January 1 is week '01')  
NNN Alphanumeric traceability code  
(e3) Pb-free JEDEC® designator for Matte Tin (Sn)  
\* This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

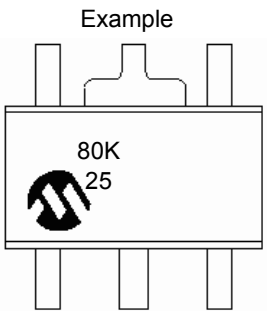
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# MCP1804

---



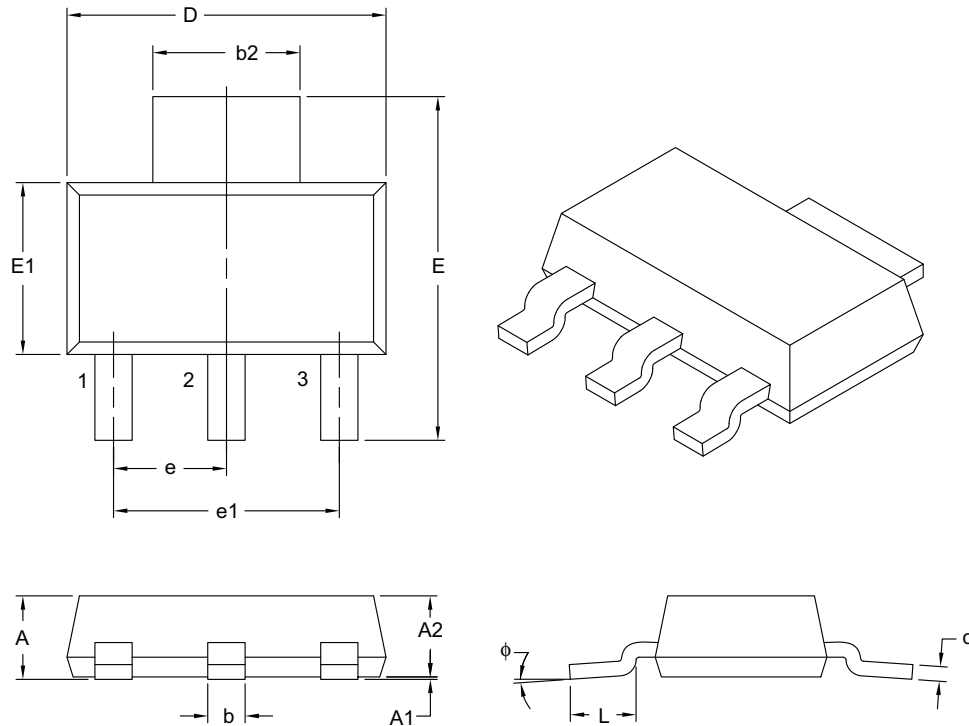
Part Number	Code
MCP1804T-1802I/MT	80KXX
MCP1804T-2502I/MT	80TXX
MCP1804T-3002I/MT	80ZXX
MCP1804T-3302I/MT	812XX
MCP1804T-5002I/MT	81MXX
MCP1804T-A002I/MT	839XX
MCP1804T-C002I/MT	83ZXX





## 3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Leads	N	3		
Lead Pitch	e	2.30 BSC		
Outside Lead Pitch	e1	4.60 BSC		
Overall Height	A	—	—	1.80
Standoff	A1	0.02	—	0.10
Molded Package Height	A2	1.50	1.60	1.70
Overall Width	E	6.70	7.00	7.30
Molded Package Width	E1	3.30	3.50	3.70
Overall Length	D	6.30	6.50	6.70
Lead Thickness	c	0.23	0.30	0.35
Lead Width	b	0.60	0.76	0.84
Tab Lead Width	b2	2.90	3.00	3.10
Foot Length	L	0.75	—	—
Lead Angle	$\phi$	0°	—	10°

**Notes:**

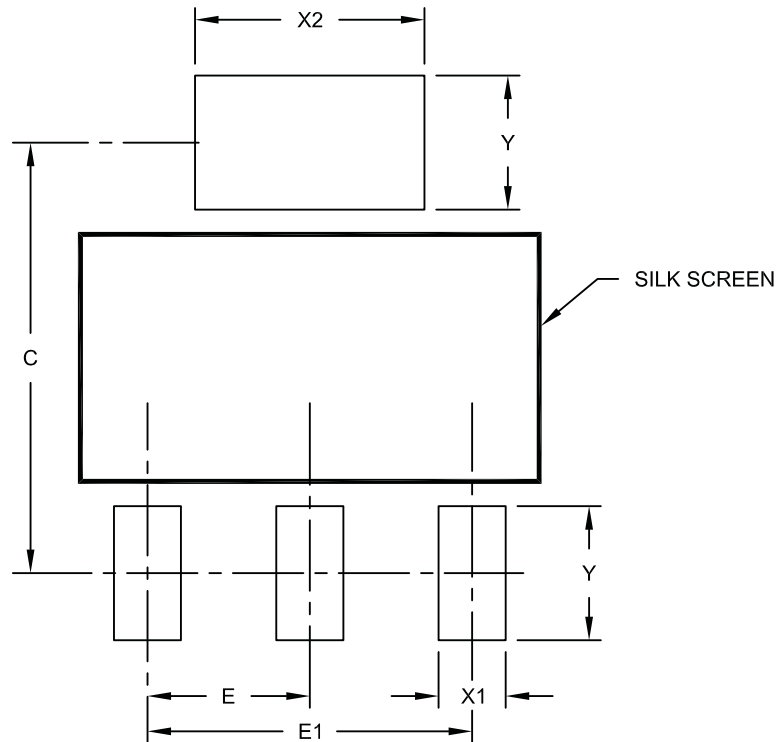
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
  - Dimensioning and tolerancing per ASME Y14.5M.
- BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

# MCP1804

## 3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.30 BSC		
Overall Pitch	E1	4.60 BSC		
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

**Notes:**

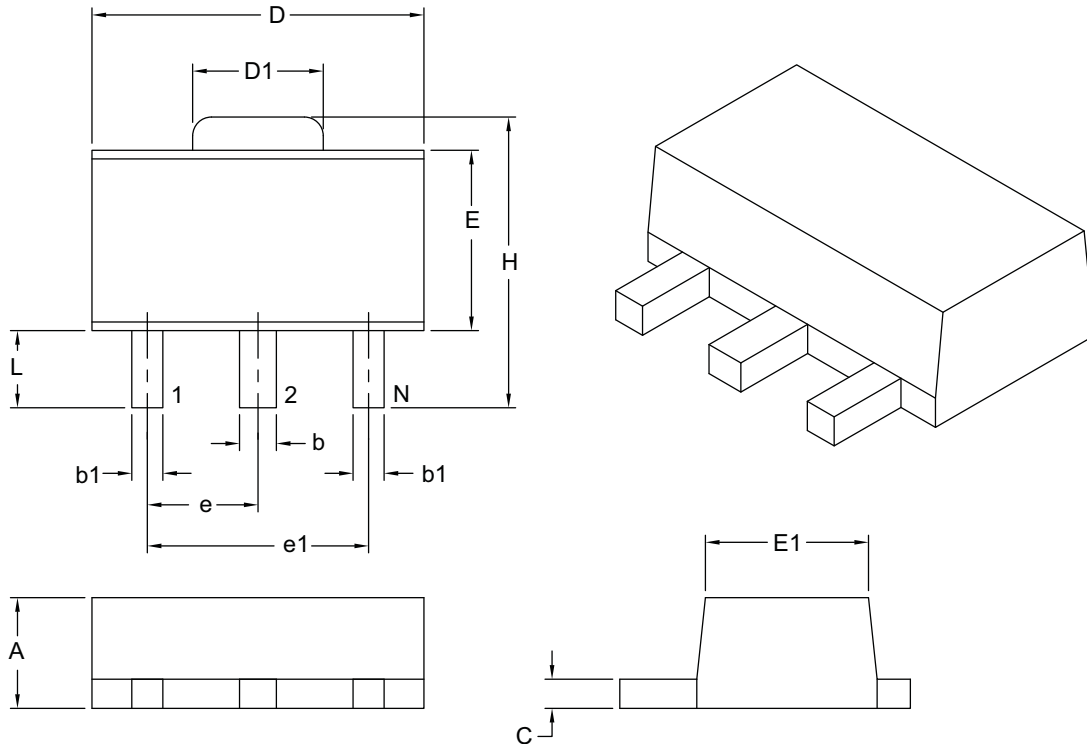
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A

## 3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



	Units	MILLIMETERS	
		MIN	MAX
Number of Leads	N	3	
Pitch	e	1.50 BSC	
Outside Lead Pitch	e1	3.00 BSC	
Overall Height	A	1.40	1.60
Overall Width	H	3.94	4.25
Molded Package Width at Base	E	2.29	2.60
Molded Package Width at Top	E1	2.13	2.29
Overall Length	D	4.39	4.60
Tab Length	D1	1.40	1.83
Foot Length	L	0.79	1.20
Lead Thickness	c	0.35	0.44
Lead 2 Width	b	0.41	0.56
Leads 1 & 3 Width	b1	0.36	0.48

**Notes:**

- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

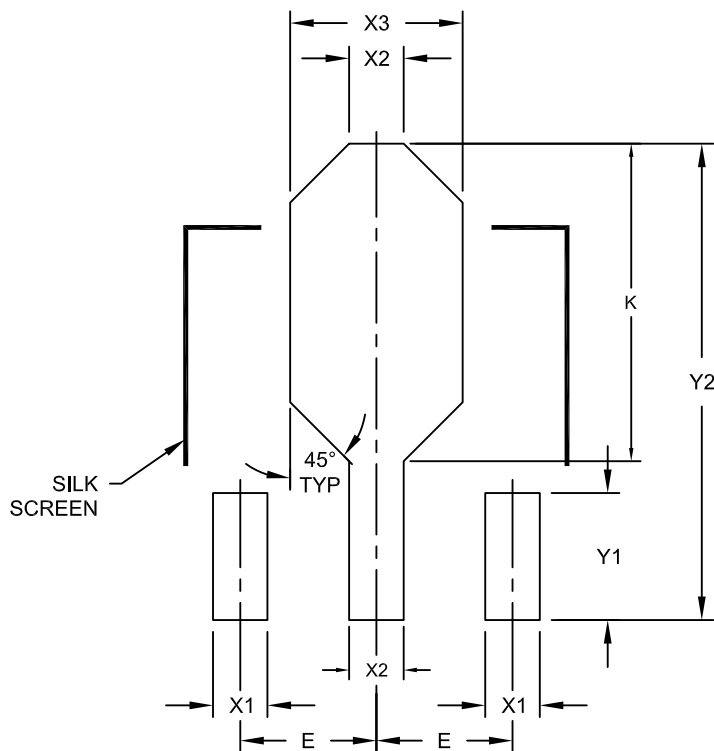
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-029B

# MCP1804

## 3-Lead Plastic Small Outline Transistor Header (MB) [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		1.50 BSC		
Contact Pads 1 & 3 Width	X1				0.48
Contact Pad 2 Width	X2				0.56
Heat Slug Pad Width	X3				1.20
Contact Pads 1 & 3 Length	Y1			1.40	
Contact 2 Pad Length	Y2				4.25
-	K		2.60		2.85

**Notes:**

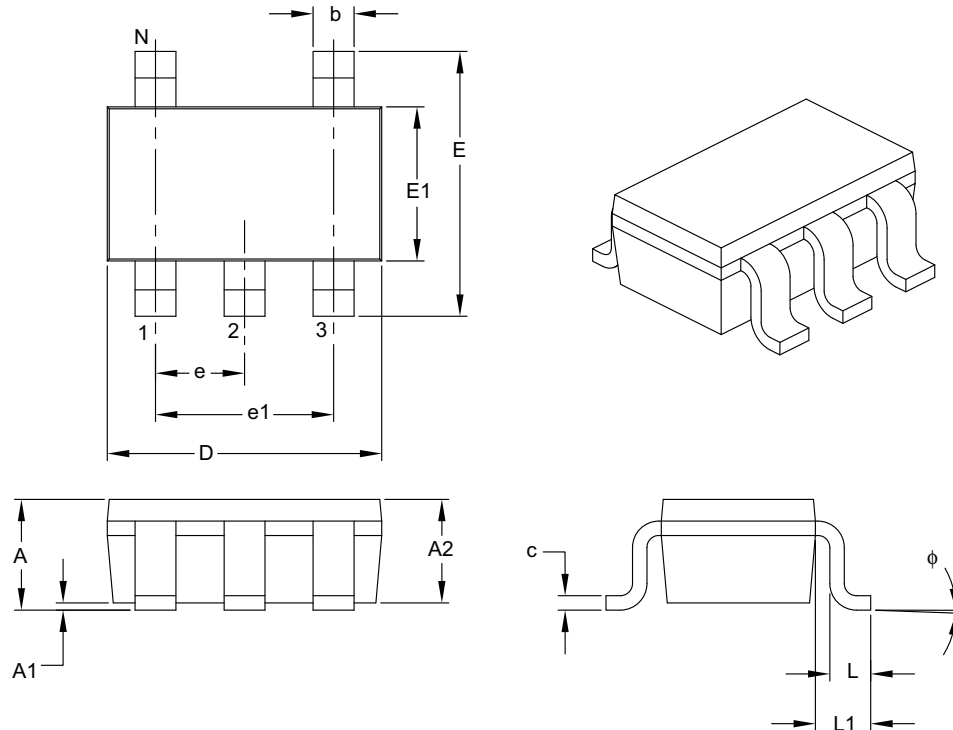
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2029A

## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Lead Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	—	1.45
Molded Package Thickness	A2	0.89	—	1.30
Standoff	A1	0.00	—	0.15
Overall Width	E	2.20	—	3.20
Molded Package Width	E1	1.30	—	1.80
Overall Length	D	2.70	—	3.10
Foot Length	L	0.10	—	0.60
Footprint	L1	0.35	—	0.80
Foot Angle	$\phi$	0°	—	30°
Lead Thickness	c	0.08	—	0.26
Lead Width	b	0.20	—	0.51

**Notes:**

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

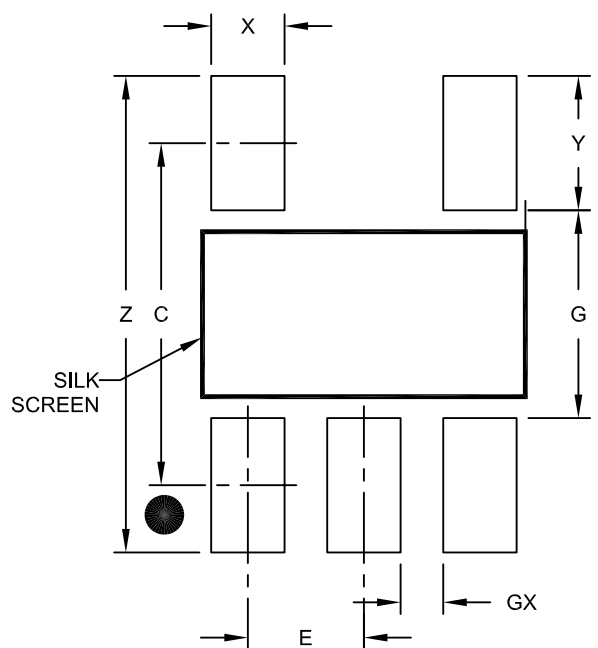
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

# MCP1804

## 5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

**Notes:**

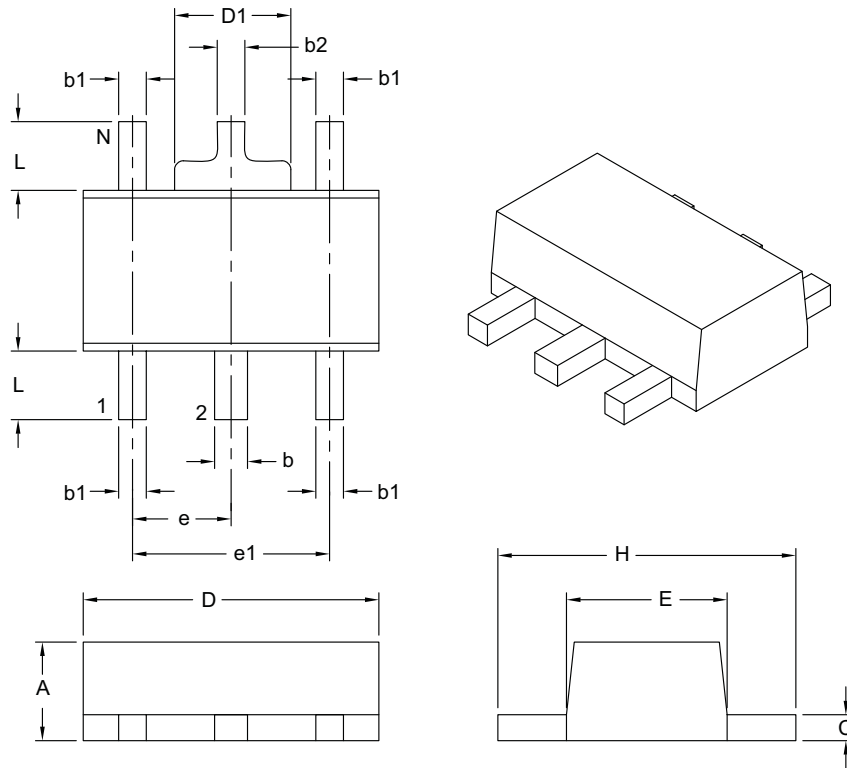
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

## 5-Lead Plastic Small Outline Transistor Header (MT) [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



	Units	MILLIMETERS	
		MIN	MAX
Number of Leads	N	5	
Lead Pitch	e	1.50 BSC	
Outside Lead Pitch	e1	3.00 BSC	
Overall Height	A	1.40	1.60
Overall Width	H	3.94	4.50
Molded Package Width	E	2.29	2.60
Overall Length	D	4.40	4.60
Tab Width	D1	1.40	1.83
Foot Length	L	0.80	1.20
Lead Thickness	c	0.35	0.44
Lead 2 Width	b	0.41	0.56
Leads 1, 3, 4 & 5 Width	b1	0.36	0.48
Tab Lead Width	b2	0.32	0.48

### Notes:

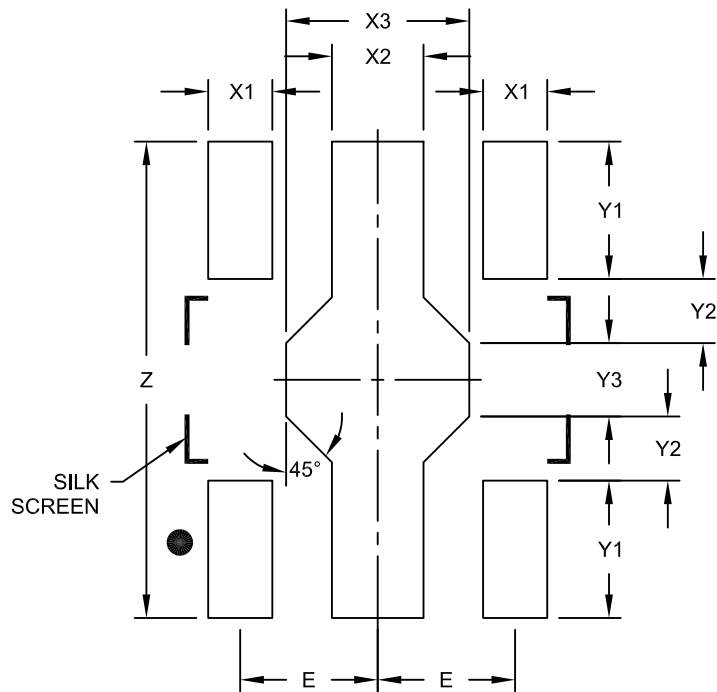
- Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-030B

## 5-Lead Plastic Small Outline Transistor Header (MT) [SOT-89]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.50 BSC		
Contact Pad Width (X4)	X1			0.70
Contact Pad Width	X2		1.00	
Contact Pad Width	X3		2.00	
Contact Pad Length (X4)	Y1		1.50	
Contact Pad Length (X2)	Y2		0.70	
Contact Pad Length	Y3		0.80	
Overall Length	Z		5.20	

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2030C



## APPENDIX A: REVISION HISTORY

### Revision D (October 2013)

The following is the list of modifications:

1. Added operating junction temperature range in [Temperature Specifications](#).
2. Updated the maximum package power dissipation values in [Section 6.3.1.2, Junction Temperature Estimate](#).
3. Updated package specification drawings to reflect all view.
4. Minor typographical changes.

### Revision C (June 2011)

The following is the list of modifications:

5. Added seven new characterization graphs to [Section 2.0, Typical Performance Curves \(Figures 2-49 - 2-55\)](#).
6. Changed layout of [Table 3-1](#). Added separate column for SOT-223-3.
7. Updated Package Marking drawings and examples in the Packaging Information section.
8. Added new voltage option to Product Identification System table.

### Revision B (November 2009)

The following is the list of modifications:

- Electrical characteristics,  $\overline{\text{SHDN}}$  "H" Voltage item: Changed to SHDN "L" Voltage.

### Revision A (September 2009)

- Original Release of this Document.

# MCP1804

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>I</u>	<u>-XX</u>	<u>XX</u>	<u>X</u>	<u>/XX</u>
Device	Tape and Reel	Voltage	Output Voltage Tolerance	Temperature Range	Package
<b>Examples:</b>					
a) MCP1804T-1802I/OT: 1.8V, 5-LD SOT-23 b) MCP1804T-2502I/OT: 2.5V, 5-LD SOT-23 c) MCP1804T-3002I/OT: 3.0V, 5-LD SOT-23 d) MCP1804T-3302I/OT: 3.3V, 5-LD SOT-23 e) MCP1804T-5002I/OT: 5.0V, 5-LD SOT-23 f) MCP1804T-A002I/OT: 10V, 5-LD SOT-23 g) MCP1804T-C002I/OT: 12V, 5-LD SOT-23					
a) MCP1804T-1802I/MB: 1.8V, 3-LD SOT-89 b) MCP1804T-2502I/MB: 2.5V, 3-LD SOT-89 c) MCP1804T-3002I/MB: 3.0V, 3-LD SOT-89 d) MCP1804T-3302I/MB: 3.3V, 3-LD SOT-89 e) MCP1804T-5002I/MB: 5.0V, 3-LD SOT-89 f) MCP1804T-A002I/MB: 10V, 3-LD SOT-89 g) MCP1804T-C002I/MB: 12V, 3-LD SOT-89					
a) MCP1804T-1802I/MT: 1.8V, 5-LD SOT-89 b) MCP1804T-2502I/MT: 2.5V, 5-LD SOT-89 c) MCP1804T-3002I/MT: 3.0V, 5-LD SOT-89 d) MCP1804T-3302I/MT: 3.3V, 5-LD SOT-89 e) MCP1804T-5002I/MT: 5.0V, 5-LD SOT-89 f) MCP1804T-A002I/MT: 10V, 5-LD SOT-89 g) MCP1804T-C002I/MT: 12V, 5-LD SOT-89					
a) MCP1804T-1802I/DB: 1.8V, 3-LD SOT-223 b) MCP1804T-2502I/DB: 2.5V, 3-LD SOT-223 c) MCP1804T-3002I/DB: 3.0V, 3-LD SOT-223 d) MCP1804T-3302I/DB: 3.3V, 3-LD SOT-223 e) MCP1804T-5002I/DB: 5.0V, 3-LD SOT-223 f) MCP1804T-A002I/DB: 10V, 3-LD SOT-223 g) MCP1804T-C002I/DB: 12V, 3-LD SOT-223					

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.


Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICTail, REAL ICE, rLAB, Select Mode, SQL, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2009-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-62077-590-5

**QUALITY MANAGEMENT SYSTEM**  
**CERTIFIED BY DNV**  
**== ISO/TS 16949 ==**

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*



## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Farmington Hills, MI  
Tel: 248-538-2250  
Fax: 248-538-2260

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**Santa Clara**  
Santa Clara, CA  
Tel: 408-961-6444  
Fax: 408-961-6445

**Toronto**  
Mississauga, Ontario,  
Canada  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2401-1200  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-2819-3187  
Fax: 86-571-2819-3189

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7828  
Fax: 886-7-330-9305

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**UK - Wokingham**  
Tel: 44-118-921-5869  
Fax: 44-118-921-5820

08/20/13

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

## Microchip:

<a href="#"><u>MCP1804T-1802I/DB</u></a>	<a href="#"><u>MCP1804T-1802I/MB</u></a>	<a href="#"><u>MCP1804T-1802I/MT</u></a>	<a href="#"><u>MCP1804T-1802I/OT</u></a>	<a href="#"><u>MCP1804T-2502I/DB</u></a>
<a href="#"><u>MCP1804T-2502I/MB</u></a>	<a href="#"><u>MCP1804T-2502I/MT</u></a>	<a href="#"><u>MCP1804T-2502I/OT</u></a>	<a href="#"><u>MCP1804T-3002I/DB</u></a>	<a href="#"><u>MCP1804T-3002I/MB</u></a>
<a href="#"><u>MCP1804T-3002I/MT</u></a>	<a href="#"><u>MCP1804T-3302I/DB</u></a>	<a href="#"><u>MCP1804T-3302I/MB</u></a>	<a href="#"><u>MCP1804T-3302I/MT</u></a>	<a href="#"><u>MCP1804T-3302I/OT</u></a>
<a href="#"><u>MCP1804T-5002I/DB</u></a>	<a href="#"><u>MCP1804T-5002I/MB</u></a>	<a href="#"><u>MCP1804T-5002I/MT</u></a>	<a href="#"><u>MCP1804T-5002I/OT</u></a>	<a href="#"><u>MCP1804T-A002I/DB</u></a>
<a href="#"><u>MCP1804T-A002I/MB</u></a>	<a href="#"><u>MCP1804T-A002I/MT</u></a>	<a href="#"><u>MCP1804T-A002I/OT</u></a>	<a href="#"><u>MCP1804T-C002I/DB</u></a>	<a href="#"><u>MCP1804T-C002I/MB</u></a>
<a href="#"><u>MCP1804T-C002I/MT</u></a>	<a href="#"><u>MCP1804T-C002I/OT</u></a>			